DATA SHEET

PCF7941ATJ

PCF7341ATJ

Security Transponder and RISC Controller (STARC 2XLite)

Product Specification

2013 Oct 15

CONFIDENTIAL

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1 FEATURES

- Single chip Security Transponder and Remote Keyless Entry solution
- RISC programmable device features
- Up to seven Keyless Entry command buttons
- 512 Byte EEPROM for extended data storage
- 32 bit unique device and product type identification
- Package integrated Transponder LF coil

Security Transponder

- Transponder operation like PCF7936 family
- Fast mutual authentication, 39ms (48 bit Secret Key)
- EEPROM read/write protection capability
- RISC programmable transponder extensions

Calculation Unit

- Hardwired security algorithm
- 48 (96) bit Secret Key

RISC Controller and Peripherals

- 8 Bit RISC Architecture (MRK II)
- 4 kByte E-ROM respectively ROM (application)
- 4 kByte ROM (device firmware and library functions)
- 128 Byte User RAM
- 11 general purpose I/O (incl. 7 command button inputs)
- Two 8 Bit Timer/Counter
- Optional external clock input for Timer/Counter
- Watchdog
- Single level interrupt architecture
- On-chip RC Oscillator (< ±8%)
- Short instruction execution time (as fast as 0.5 μs)
- Programmable battery low detection
- Low power consumption
  RUN: 300 μA, IDLE: 20μA, PD: 100 nA
- Single Lithium cell operation, 2.1V to 3.6V

2 GENERAL DESCRIPTION

The PCF7x41ATJ is a high performance single chip Security Transponder and RISC Controller, ideally suited for automotive applications with combined vehicle Immobilization and Remote Keyless Entry functions.

Unless other products, the device comes with a package integrated Transponder LF coil to operate as Security Transponder and enable contactless communication with the base station. Neither other external components nor an additional battery supply is needed. The basic transponder operation is emulated utilizing the on-chip RISC and may feature a customized functions or may utilize the built in Transponder Library, that offer HT2 functional compatible operation (e.g. PCF7936), except for the ReadOnly mode.

The Security Transponder operation features secure contactless authentication, employing a Secret Key and a random number in order to cipher any communication between the device and the base station. The device features a factory programmed unique serial number that also serves as product type identification.

Device operation is controlled by a ROM or E-ROM (FLASH like features) based RISC Controller, powered by NXP' low power 8-Bit MICRO RISC KERNEL (MRK II). 11 general purpose I/Os are provided for command buttons, LED, or control of an external RF transmitter/transceiver circuitry.

In case of Remote Keyless Entry applications, the application program may accomplish rolling code generation using the hardwired Calculation Unit. The Calculation Unit may operate in standard HITAG2 (48 bit Shift Register) or Enhanced mode (64 bit Shift Register).

The RISC employs a 2 stage pipeline architecture in order to execute an instruction in a single clock cycle. Device timing is derived from an on-chip low tolerance RC Oscillator that provides a programmable system clock, with a frequency up to 2 MHz. The system clock may also be derived from the transponder interface, e.g. LF field clock.

Depending on the operation mode, the RISC is powered from the external battery or derives its power supply by inductive coupling to the LF field generated by the base station.

The PCF7x41ATJ incorporates an advanced power management that supports battery voltage measurement. For increased battery lifetime the device quiescent current is minimized in POWER-OFF state by disconnecting the battery from most of the internal circuitry.

The device comes in a 36 pin Leaded Stick Package (LSP). The device is available as E-ROM (FLASH like features) and ROM coded product. In case of the E-ROM version, in-circuit program download and debugging is supported.

For further detailed descriptions about features, functional blocks and known anomalies not related to the integrated Transponder functionality, please refer to datasheet PCF7x41A compiled for the SSOP and TSSOP package.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	OUTLINE VERSION	
PCF7941ATJ/CA1B00E0	SOJ36	Leaded Stick Package	SOT867-1	-40°C to +85°C
PCF7941ATJ/CA1Brrff	SOJ36	Leaded Stick Package	SOT867-1	-40°C to +85°C
PCF7341ATJ/C0ABrrff	SOJ36	Leaded Stick Package	SOT867-1	-40°C to +85°C

Note

1. PCF7941ATJ/CA1B00E0 represents the E-ROM product for development and applications with low quantities. The customer shall perform E-ROM programming and EEPROM initialization. The Monitor and Download Interface (MSDA/MSCL) supports E-ROM download and ERASE/WRITE as fast as 700ms for 4 kByte.
2. PCF7941ATJ/CA1Brrff represents a customized E-ROM product. Under certain conditions NXP Semiconductors may perform E-ROM programming with a customer application code and/or customer EEPROM pattern. The actual customer application code and customer EEPROM fabkey is specified by a 2 digit code at location marked “ff”. The ROM code is specified by a 2 digit code at location marked „rr“
2. PCF7341ATJ/C0ABrrff represents the ROM coded product for high volume applications. The actual customer ROM code and customer EEPROM fabkey is specified by a 2 digit code at location marked „rr“, respectively “ff”

4 TYPICAL APPLICATION

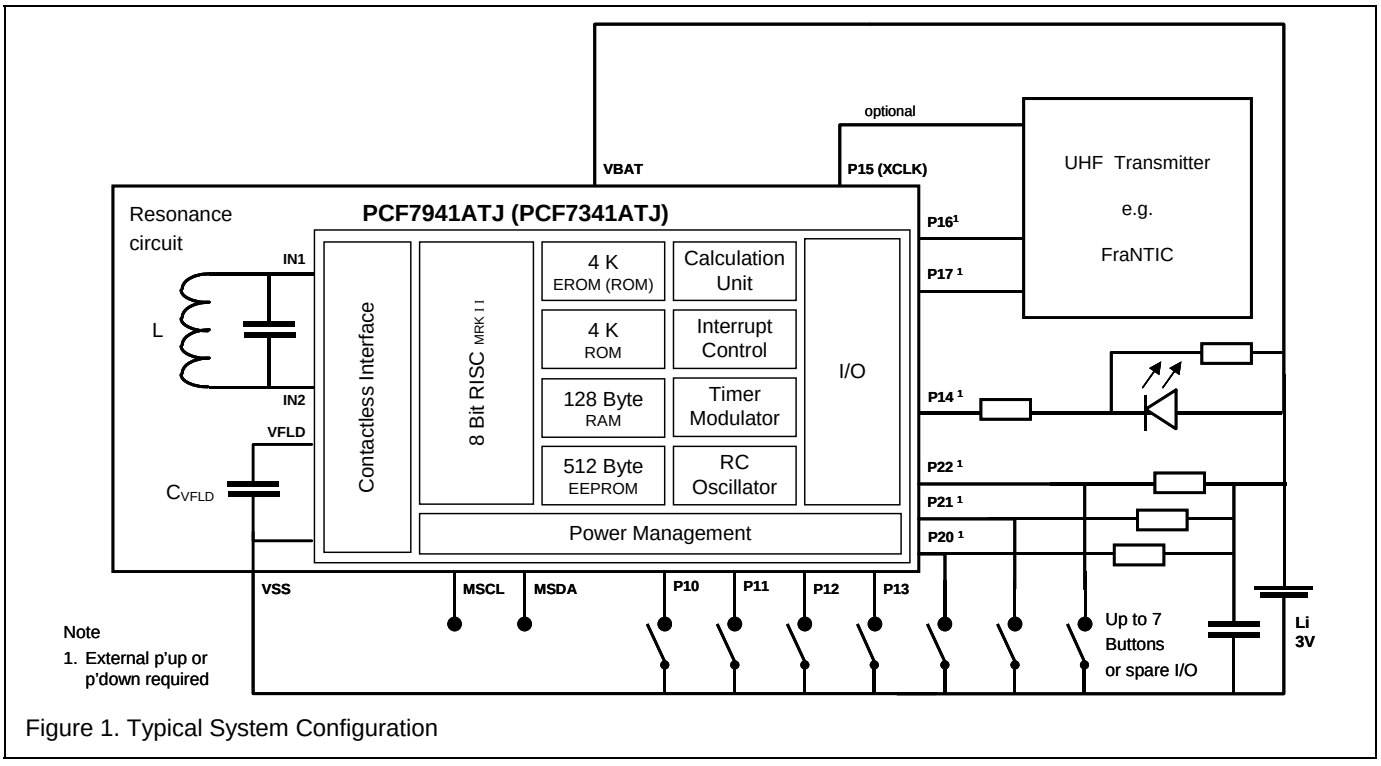


Figure 1. Typical System Configuration

5 BLOCK DIAGRAM

The PCF7x41ATJ features a high degree of integration and incorporates the chip, coil and capacitors assembled in a leaded stick package, see Figure 2.

Package

- L/C Resonance Circuit
- Rectified LF Filed supply blocking capacitor

Contactless Interface

- Rectifier and Voltage Limiter
- Modulator
- Clock Recovery
- Demodulator
- LF Field Detection

Calculation Unit

- HT2 (48 bit) and HT3 (96 bit) Algorithm

Power Management

- Supply Switch Logic
- Wake Up Sense (Button I/O)
- Watchdog Timer
- Reset Logic

RISC Controller and Peripherals

- 8 Bit RISC (MRK II)
- ROM (Firmware)
- E-ROM (Application program)
- RAM
- EEPROM
- Interrupt Control
- Timers / Counters
- I/O Ports
- Programmable Voltage Comparator
- System Clock (including on-chip RC oscillator)

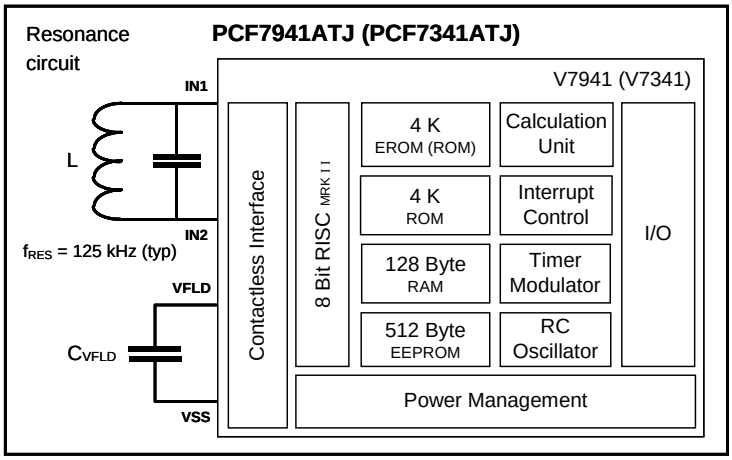


Figure 2. Block Diagram

6 QUICK REFERENCE DATA

6.1 Transponder Operation

PARAMETER	VALUE	UNIT
Carrier frequency	125	kHz
Data rate - read - write	 4.0 5.2	 kbit/s kbit/s
Data coding - read - write	 Manchester or Bi-Phase Binary Pulse Length Modulation (BPLM)	
Data transmission mode	Half-Duplex	
Modulation	Amplitude Shift Keying (ASK)	

6.2 RISC Controller and Peripherals

PARAMETER	VALUE	UNIT
Operating supply voltage (RISC)	2.1 - 3.6	V
Power-down current (typical)	400	nA
ROM (Firmware – System ROM)	4 K	Byte
E-ROM (Application program)	4 K	Byte
RAM	128	Byte
EEPROM	512	Byte
General purpose /O	11	
Operating speed, as derived from on-chip RC oscillator	0.125 - 2	MHz

Special Features	• EEPROM Erase/Write over full operating voltage range (2.1 to 3.6 V) • Full control about Contactless LF Interface • Programmable voltage comparator for battery voltage monitoring • PWM generation • Watchdog timer • Up to 7 dedicated Wake-Up button inputs
Calculation Unit	• Features HT2 (48 bit) or HT3 (96 bit) • Supports Pseudo Random Number generation (Rolling Code)

7 PINNING

Table 1. Pin Assignment

FUNCTION	DESCRIPTION	PIN	NOTE
i.c. A	Internally connected (node reference A)	1	2
i.c. A	Internally connected (node reference A)	2	2
i.c. A	Internally connected (node reference A)	3	2
VSS	Common Ground digital section (Battery neg. Terminal)	4	
n.c.	Not connected	5	1
n.c.	Not connected	6	1
n.c.	Not connected	7	1
P20	General purpose I/O, Wake Up sense and Digital modulator output	8	
P16	General purpose I/O, voltage comparator input	9	
P17	General purpose I/O, Digital modulator outpu	10	
P15	General purpose I/O and external clock input	11	
P10	General purpose I/O with internal pull-up, Wake Up sense	12	
P21	General purpose I/O, Wake Up sense and Timer 1 Capture input / Interrupt input	13	
n.c.	Not connected	14	
i.c. B	Internally connected (node reference B)	15	3
n.c.	Not connected	16	
MSDA	ROM Monitor Serial Data with internal pull-up	17	4
i.c. C	Internally connected (node reference C)	18	2
i.c. C	Internally connected (node reference C)	19	2
MSCL	ROM Monitor Serial Clock Output	20	
n.c.	Not connected	21	
n.c.	Not connected	22	
P22	General purpose I/O, Wake Up sense and Timer 1 Compare output (PWM)	23	
P11	General purpose I/O with internal pull-up and Wake Up sense	24	
P12	General purpose I/O with internal pull-up and Wake Up sense	25	
P13	General purpose I/O with internal pull-up and Wake Up sense	26	
TEST	Reserved	27	1
TEST	Reserved	28	1
TEST	Reserved	29	1
VBAT	Battery Supply Voltage digital section (Battery pos. Terminal)	30	
P14	General purpose I/O	31	
i.c. B	Internally connected (node reference B)	32	3
i.c. F	Internally connected (node reference F)	33	2
i.c. F	Internally connected (node reference F)	34	2
i.c. E	Internally connected (node reference E)	35	2
i.c. E	Internally connected (node reference E)	36	2

Note

1. Reserved for device test purposes. Required to be left unconnected or connected to VSS
2. Internally connected to another pin and not connected to the chip.
3. Internally connected to another pin and not connected to the chip, but connected to the chip die attach.
4. MSCL is an output and must be left unconnected in the application. MSDA features an on-chip pull-up to VBAT, and may be left open or terminated to VBAT, as desired. For details please refer to the ‘PCF7941 Monitor and Download Interface’ (see 13 RELATED DOCUMENTS).

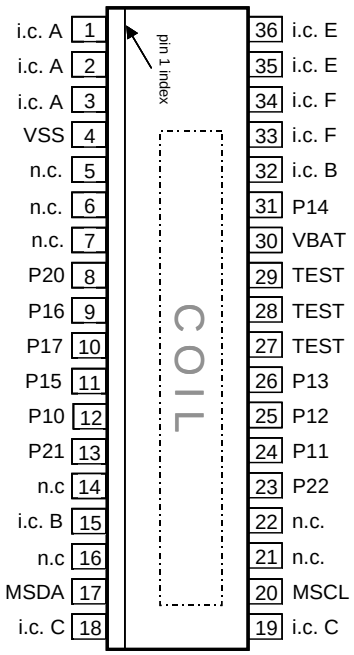


Figure 3. Pin Configuration

8 FUNCTIONAL DESCRIPTION

The PCF7x41ATJ incorporates Security Transponder and Remote Keyless Entry features that are specified in detail by the data sheet PCF7x41 and the corresponding ROM Library Description; see section 13.

8.1 LF Field Power On Reset

When the transponder enters a LF Field a rectifier circuitry becomes operational and the rectified voltage develops. The LF Field has to be present for at least 2ms ($t_{FLD,HLD}$) before this supply voltage is passed on to become the transponder supply voltage (V_{DDC}). As soon as the supply voltage (V_{DDC}) exceeds the LF Field Power-On Reset threshold voltage ($V_{POR,FLD}$) the device performs a chip reset and starts its initialization sequence by executing its boot routine, see Figure 4.

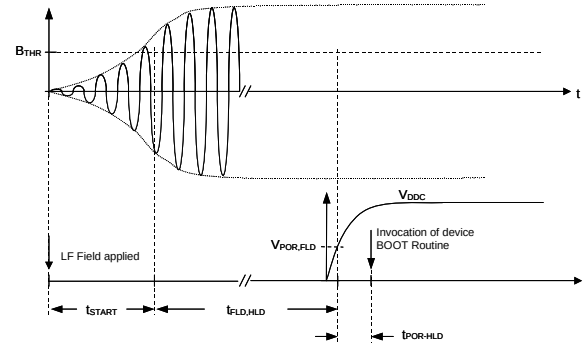


Figure 4 LF field power on reset timing

Subsequently, the transponder is muted and does not respond to any command until termination of the device boot sequence. The startup time, t_{START}, depends on the base station configuration, the resonance circuit properties and the system coupling factor, however, is small compared with the LF Field hold time ($t_{FLD,HLD}$).

Regardless of the supply condition, once the supply voltage (VDD) exceeds the Power On Reset threshold voltage (VPOR,BAT respectively VPOR,FLD), POR becomes low. After a short delay (TPOR,HLD), the flip-flop is forced into latch state freezing the supply switch state and the RISC Controller becomes operational. Program execution commences starting with the BOOT Routine, before the application Program or Transponder Emulation is being invoked, see Figure 5

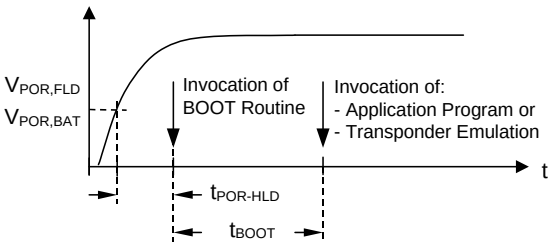


Figure 5 Power-up timing

In order to force a LF Field Power-On Reset and proper device initialization at any time, the LF field OFF condition must be applied for at least $t_{RESET,SETUP}$, in order to ensure that the INTERNAL device supply voltage, V_{DDc}, drops below the threshold voltage ($V_{POR,FLD}$), see Figure 6.

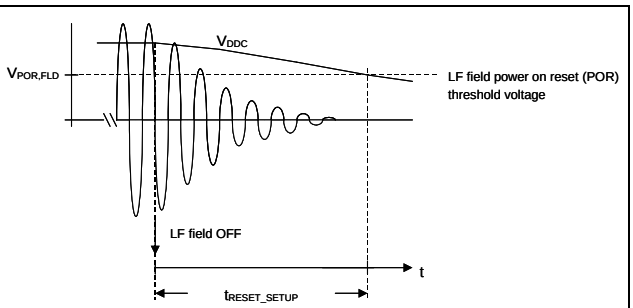


Figure 6 LF field power on reset setup timing

9 EEPROM CONTENT AT DELIVERY

The PCF7x41ATJ EEPROM content is initialized during device manufacturing, according to Table 2.

However the EEPROM content may be modified as desired by the application, except for the page 0 block 0 which holds the Identifier (IDE) and serves the function of a serial number and product type ID.

Table 2. EEPROM Content Upon Delivery

Content [HEX]	Page	Note
XX XX XX 6X	0	1
4D 49 4B 52	1	
00 00 4F 4E	2	
00 AA 48 54	3	
XX XX XX XX	4 to 126	
X6 XX 80 00	127	

MSB LSB

Note

1. Bit 7 to 4 of this page (Identifier) serve the function of a product type (application) identifier and are set to ‘0110’ for the PCF7x41ATJ. For system compatibility reasons, the same product type Identifier is used by PCF7x21 (KEECOR).
2. Locations marked ‘X’ are undefined and may hold any pattern.

Consequently, the device is configured for PCF7936 (HITAG2) transponder emulation and set to INIT mode, providing full support regarding the Monitor and Download Interface.

10 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134)

PARAMETER	MIN	MAX	UNIT
Operating temperature range	-40	+85	°C
Storage temperature range	-55	+125	°C
Reflow soldering peak temperature, Note 2		232,5	°C
Package Mositure Sensitivity Level (MSL)		3	
Magnetic flux density (resistance against magnetic pulses)		0.2	T
Latch-up current, Note 3	100		mA
ESD, human body model, Note 4	2		kV
ESD, human body model for pins VBAT and VSS, Note 4	4		kV
ESD, machine model, Note 5	250		V
ESD CDM, Field Induced Model for corner pins, Note 6	750		V
ESD CDM, Field Induced Model for all pins besides corner pins, Note 6	650		V
Vibration - 10 - 2000Hz - 3.axis - IEC 68-2-6, Test Fc		10	g
Shock - 3.axis - IEC 68-2-27, Test Ea		1500	g
Mechanical stress (F_{MAX}), Note 1		10	N

Note

1. F_{MAX} is specified as indicated in Test Setup, section 12.
2. Reflow stress levels in accordance with JEDEC 22 A113D, excluding limitation of peak temperature.
3. According to JEDEC, JESD 17.
4. According to JEDEC, JESD 22-A114.
5. According to JEDEC, JESD 22-A115.
6. According to JEDEC, JESD 22-C101.

11 DEVICE CHARACTERISTICS

11.1 Electrical Characteristics

Tamb = -40 to +85°C, f_{SYS} = 125kHz, $T_O = 1/f_{SYS}$. Unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Operating Conditions						
C_{VFLD}	Supply blocking capacitor			22		nF
L	Transponder coil inductance			4.8		mH
f_{RES}	Resonance frequency		119		131	kHz
BW	Bandwidth		2.3			kHz
B_{THR}	Magnetic flux density, Read direction		60		400	μT_{PP}
B_{PRG}	Magnetic flux density for EEPROM programming	m = 0,95, T_{WRP} = 8 T_O Note 1	60		400	μT_{PP}
B_{AUT}	Magnetic flux density for device authentication	m = 0,95, T_{WRP} = 8 T_O Note 1	60		400	μT_{PP}
B_{READ}	LF field absorption in read direction, Note 1	B_{FIELD} = 60 μT_{PP}	4.5			μT_{PP}
MI_{PRG}	Minimum modulation index (m) Write direction (device programming and authentication).	B_{FIELD} = 60 μT_{PP}, T_{WRP} = 8 T_O Note 1			95	%

Note

1. Modulation index (m) and LF Field absorption (B_{READ}) are defined according to Figure 7.
2. Parameters are measured with the Scemtech test equipment STM-1 in a Helmholtz arrangement according to section 12.
3. Typical temperature dependency of bandwidth BW shown in Figure 8.

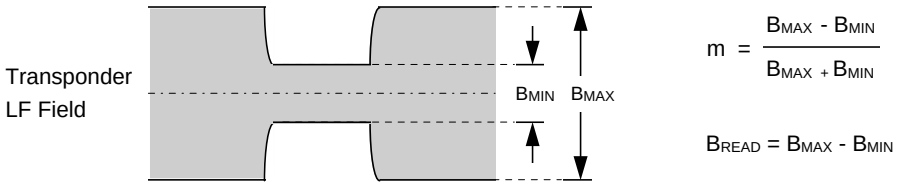


Figure 7. Definition of modulation index (m) and LF field absorption (B_{READ})

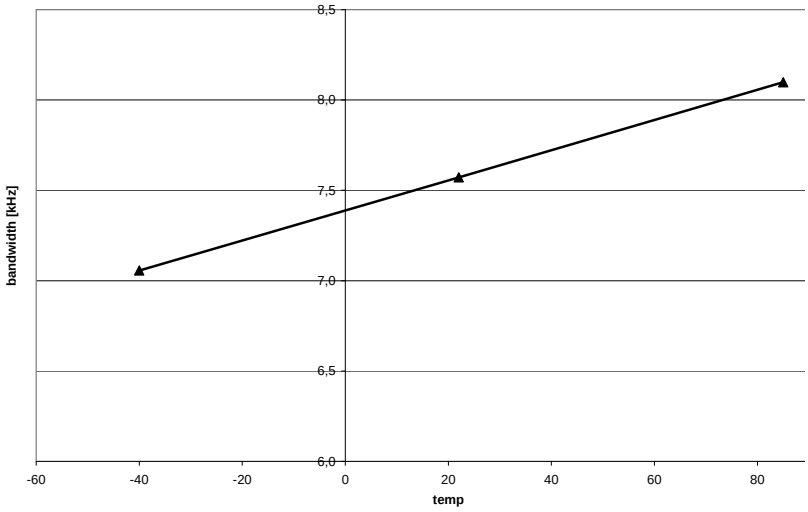


Figure 8 Typical temperature dependency of bandwidth BW

11.2 Timing Characteristics

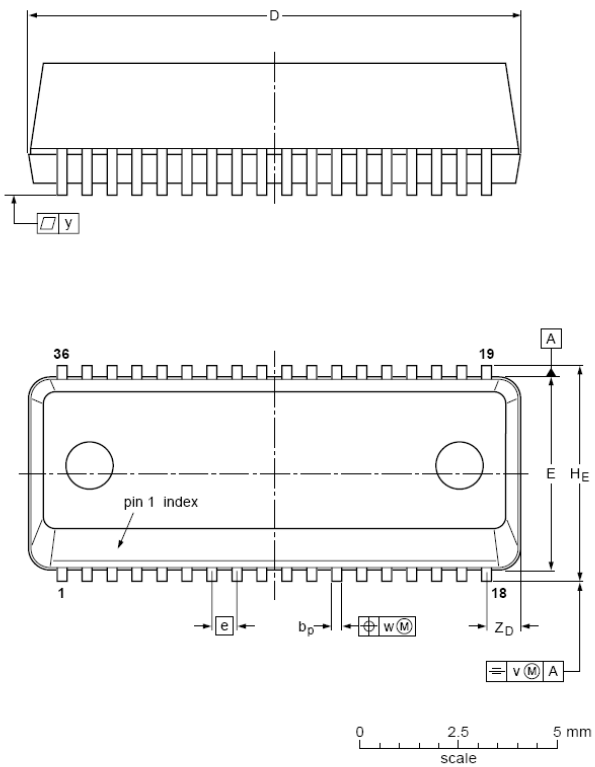
Tamb = -40 to +85°C, f_{SYS} = 125kHz, $T_O = 1/f_{SYS}$. Unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
LF Field Power On Reset, Note 1						
$t_{FLD,HLD}$	LF Field hold time		250			T_O
$t_{POR-HLD}$	Power On Reset Hold time			200	480	µs
$t_{RESET,SETUP}$	LF Field Power On Reset setup time		11			ms

Notes

1. Values based on PCF7x41A PQP with additional safety margin considering application of LSP resonance circuit.

11.3 Mechanical Characteristics



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_E	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	θ
mm	3.5	0.45 0.15	3.2 2.8	0.25	0.3 0.2	0.15	12.65 12.35	5.0 4.8	0.635	4.94	5.6 5.4	0.35	1.08 0.48	2.2 2.0	0.2	0.13	0.1	1.1 0.6	15° 0°

Figure 9. Package outline SOT 867-1

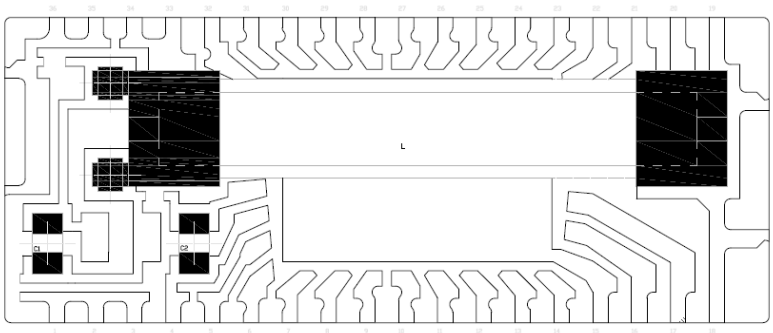


Figure 10. Coil position, SOT 867

12 TEST SETUP

Device characteristics are measured according to the test setups given below.

Electrical characteristics are measured in a Helmholtz arrangement that generates an almost homogenous magnetic field at the position of the device under test (transponder); see Figure 12.

The sense coils detect the absorption modulation induced by the transponder, whereas the reference coils sense the magnetic flux generated by the field generating coils only. The voltage difference measured between the sense coils and reference coils is proportional to the magnetic field absorption induced by the transponder.

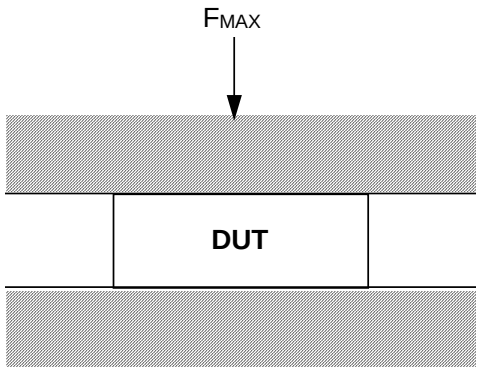


Figure 11. Mechanical Stress

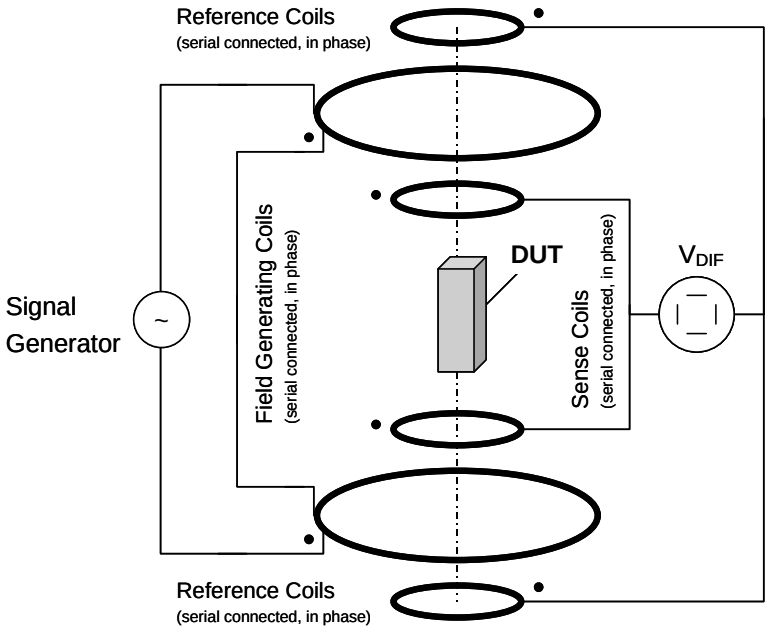


Figure 12. Helmholtz setup for electrical characteristics

13 RELATED DOCUMENTS

Type	Name / Reference	Description
Data Sheet	PCF7941 / PCF7341	Product Specification
Data Sheet	PCF7x41 ROM Library	Implementation and Description
Data Sheet	PCF7941 Monitor and Download Interface	Functional Description

14 DEVELOPMENT TOOLS

Reference	Name	Description
OM6710	RIDE	Software development suite
OM6713	Universal Download and Debug Board (U-DDB)	Hardware and software Interface between host PC and target device.
OM6714	EWMRKII (Embedded workbench for MRKII microcontroller cores)	New Software development suite with C-compiler and for emulation
OM6715	2LINK hardware	USB connection with emulation electronic for OM6714

15 REVISION HISTORY

Revision	Page	Description
2006 Apr 24		Objective Specification
2006 Jul 19		Editorial changes and correction LIMITING VALUES updated
	11	+ Moisture Sensitivity Level fixed to MSL 2
2007 Jun 20	all	Editorial changes and correction
	11	+ Moisture Sensitivity Level fixed to MSL 3 + Table 11.1 Electrical Characteristics: Magnetic flux density MIN values adapted
2007 Nov 1	9	Inserted Chapter 8.1 LF Field Power On Reset Product specification release
2011 Aug 10		Editorial changes
	17	Update Legal Information.
2013 Oct 15	4	Update ORDERING INFORMATION.

16 LEGAL INFORMATION

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft

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17 Contact information

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